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Approved for use through 10/31/2002. OMB 0651-0032
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. 1.53(b))

Attorney Docket No.	2207/12665
First Inventor	Gilroy J. Vandentop
Title	Electrical/Optical Integration Scheme Using Direct Copper Bonding
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☒ Fee Transmittal Form (e.g., PTO/SB/17) *(Submit an original and a duplicate for fee processing)*
2. ☐ Applicant claims small entity status. See 37 CFR 1.27.
3. ☒ Specification [*Total Pages* 19] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. ☒ Drawing(s) (*35 U.S.C.113*) [*Total Sheets* 4]
5. Oath or Declaration [*Total Pages* 2]
   a. ☒ Newly executed (original or copy)
   b. ☐ Copy from a prior application (37 CFR 1.63 (d)) *(for a continuation/divisional with Box 18 completed)*
      i. ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. ☐ Application Data Sheet. See 37 CFR 1.76
7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
8. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. ☐ Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ paper
   c. ☐ Statements verifying identity of above copies

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

ACCOMPANYING APPLICATIONS PARTS

9. ☐ Assignment Papers (cover sheet & document(s))
10. ☐ 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* ☐ Power of Attorney
11. ☐ English Translation Document *(if applicable)*
12. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
13. ☐ Preliminary Amendment
14. ☒ Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. ☐ Nonpublication Request under 35 U.S.C. 122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent.
17. ☐ Other:

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:*

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: _____ /

Prior application information: *Examiner* _____ *Group / Art Unit:*

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

☒ *Customer Number or Bar Code Label* 23838 *(Insert Customer No. or Attach bar code label here)* or ☐ *Correspondence address below*

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City		*State*		*Zip Code*	
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Name (Print/Type)	B. Delano Jordan	*Registration No. (Attorney/Agent)*	43,698
Signature		*Date*	December 19, 2001

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FEE TRANSMITTAL for FY 2002

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 1,004.00

Complete if Known	
Application Number	Unassinged
Filing Date	Herewith
First Named Inventor	Gilroy J. Vandentop
Examiner Name	Unassigned
Group / Art Unit	Unassigned
Attorney Docket No.	2207/212665

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: 11-0600

Deposit Account Name: Kenyon & Kenyon

☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1 17

☐ Applicant claims small entity status. See 37 CFR 1.27

2. ☐ Payment Enclosed:

☐ Check ☐ Credit card ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	740	201	370	Utility filing fee	740.00
106	330	206	165	Design filing fee	
107	510	207	255	Plant filing fee	
108	740	208	370	Reissue filing fee	
114	160	214	80	Provisional filing fee	

SUBTOTAL (1) ($) 740 00

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below	=	Fee Paid
Total Claims	30	-20 ** =	10	X	18	=	180
Independent Claims	4	-3 ** =	1	X	84	=	84
Multiple Dependent				X		=	0

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple dependent claim, if not paid
109	84	209	42	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 264 00

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	920	217	460	Extension for reply within third month	
118	1,440	218	720	Extension for reply within fourth month	
128	1,960	228	980	Extension for reply within fifth month	
119	320	219	160	Notice of Appeal	
120	320	220	160	Filing a brief in support of an appeal	
121	280	221	140	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive – unavoidable	
141	1,280	241	640	Petition to revive – unintentional	
142	1,280	242	640	Utility issue fee (or reissue)	
143	460	243	230	Design issue fee	
144	620	244	310	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Processing fee under 37 CFR 1 17 (q)	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	740	246	370	Filing a submission after final rejection (37 CFR § 1 129(a))	
149	740	249	370	For each additional invention to be examined (37 CFR § 1.129(b))	
179	740	279	370	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	
				Other fee (specify)	

*Reduced by Basic Filing Fee Paid **SUBTOTAL (3)** ($)

SUBMITTED BY				Complete *(if applicable)*	
Name (Print/Type)	B Delano Jordan	*Registration No Attorney/Agent)*	43,698	*Telephone*	(202) 220-4275
Signature				*Date*	12/19/01

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ELECTRICAL/OPTICAL INTEGRATION SCHEME USING DIRECT COPPER BONDING

BACKGROUND OF THE INVENTION

Technical Field

[0001] The present invention generally relates to semiconductor packages. More particularly, the invention relates to a semiconductor package and fabrication method that uses direct copper bonding to enhance performance and provide electro-optic connectivity.

Discussion

[0002] In the highly competitive computer industry, the trend toward higher processing speeds and increased functionality is well documented. While this trend is desirable to the consumer, it presents significant challenges to circuit designers as well as manufacturers. A particular area of concern relates to the design of semiconductor packages.

[0003] In a typical computing environment, an integrated circuit (IC) such as a processor is encapsulated in a dielectric material to form a semiconductor die (or IC wafer). The IC wafer often has various IC contact pads that connect to the components of the IC by way of vertically extending vias and horizontally extending wires or traces. In order to electrically connect the closely spaced IC contact pads to the various traces of an adjacent printed wiring board (PWB) such as a motherboard, a number of techniques have been used. One approach is to connect an intermediate wafer such as a chip interposer or host wafer to the IC wafer in order to form a larger and more manageable semiconductor package. The intermediate wafer has one or more intermediate contact pads providing through-connection to the board side of the intermediate wafer. Metalized vias are typically used to provide the above-described through-connection.

One conventional approach to connecting the two wafers is to use an indirect connection approach such as controlled collapse chip connection (C4). If the intermediate wafer has a socketable interconnection mechanism such as pins or ball grid array (BGA) balls, the semiconductor package can be directly mated with a socket that is hardwired to the PWB. Otherwise, a socketable interface is disposed between the semiconductor package and the socket. As processing speeds continue to increase and computing devices continue to shrink in size, the effects of packaging designs on signal throughput have drawn more attention.

[0004] One of the more recent developments has been to capitalize upon the bandwidth advantages provided by transmitting signals in the optical domain. Specifically, it has been determined that the use of optics to transfer high speed clock signals as well as input/output (I/O) signals can significantly enhance performance. Conventional semiconductor packages that make use of optics often provide an IC wafer and an intermediate wafer that has an optical arrangement. The optical arrangement will typically include a waveguide and a coupler such as a Bragg grating. The waveguide and coupler therefore provide a mechanism for transporting optical signals between an optical source such as a laser or light emitting diode (LED) and the adjacent IC wafer. It is important to note, however, that processing of the signal often occurs in the electrical domain. This is particularly true in the case of computer processors widely used in the industry. In such cases, it is common to provide a photodetector on the IC wafer that is aligned with the optical coupler during the fabrication process.

[0005] While the above-described conventional approach has been satisfactory in some circumstances, certain difficulties remain. One particular difficulty relates to the placement of the optical detector on the IC wafer. Specifically, it has been determined that C4 bonding results in a "gap" between the wafers, and that the gap can lead to a number of problems from an optical

standpoint. For example, aligning the optical arrangement with the photodetector requires a significant amount of precision in order to adequately couple the optical energy across the interface between the two wafers. Furthermore, the indirect bonding approach results in gaps on the order of 60 microns that can allow optical energy to escape regardless of how well the wafers are aligned. While the above-described optical losses could be avoided to some degree by placing the optical detector on the intermediate wafer, it has been determined that C4 bonding can also present problems from an electrical standpoint. For example, unwanted interconnect delay, resistance, capacitance, and loop inductance can all result from the C4 balls that are disposed between the IC contact pads and the intermediate contact pads. Thus, manufacturers and designers of conventional electro-optic semiconductor packages are faced with the difficult choice between the optical losses associated with IC wafer placement of the optical detector and the electrical losses associated with intermediate wafer placement of the optical detector.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. 1 is a sectional view of an example of an electro-optic semiconductor package before direct copper bonding in accordance with one embodiment of the present invention;

[0007] FIG. 2 is a sectional view of an example of an electro-optic semiconductor package after direct copper bonding in accordance with one embodiment of the present invention;

[0008] FIG. 3 is a flowchart of an example of a method of fabricating an electro-optic semiconductor package in accordance with one embodiment of the present invention;

[0009] FIG. 4 is a flowchart of an example of a process of direct copper bonding IC contacts pads to intermediate contact pads in accordance with one embodiment of the present invention; and

[0010] FIG. 5 is a flowchart of an example of a method of fabricating an intermediate wafer in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

[0011] Embodiments of an electro-optic semiconductor package and fabrication method provide enhanced performance. In accordance with one embodiment of the fabrication method, an integrated circuit (IC) wafer having one or more IC contact pads is provided, where the IC contact pads are connected to an IC on the IC wafer. An intermediate wafer having one or more intermediate contact pads is provided, where the intermediate contact pads are connected to an electro-optic arrangement on the intermediate wafer. The method further provides for direct copper bonding the IC contact pads to adjacent intermediate contact pads such that an electro-optic semiconductor package results.

[0012] In another embodiment, a method of fabricating an intermediate wafer provides for disposing a waveguide within the intermediate wafer. An optical coupler is positioned adjacent to the waveguide within the intermediate wafer, where the coupler enables transport of an optical signal and one or more intermediate contact pads of the intermediate wafer enable transport of an electrical signal. The method further provides for positioning an electro-optic converter between the optical coupler and the intermediate contact pads such that the converter enables conversion between the optical signal and the electrical signal. The converter may be either an optical detector or an optical emitter.

[0013] Further in accordance with embodiments of the present invention, an electro-optic semiconductor package is provided. The semiconductor package includes an IC wafer having one or more IC contact pads, where the IC contact pads are connected to an IC on the IC wafer.

An intermediate wafer has one or more intermediate contact pads, where the intermediate contact pads are connected to an electro-optic arrangement on the intermediate wafer. The contact pads form a plurality of direct copper bonds.

[0014] It is to be understood that both the foregoing general description and the following detailed description are merely exemplary of the invention, and are intended to provide an overview or framework for understanding the nature and character of the invention as it is claimed. The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute part of this specification. The drawings illustrate various features and embodiments of the invention, and together with the description serve to explain the principles and operation of the invention.

[0015] Turning now to FIGS. 1 and 2, an electro-optic semiconductor package is shown before and after the bonding process, respectively. Generally, the completed semiconductor package 10 includes an IC wafer 12 having one or more IC contact pads 14. The IC contact pads 14 are connected to an IC (not shown) on the IC wafer 12 by way of vertically extending vias 16 and horizontally extending wires or traces 18. It will be appreciated that only two levels of interconnection are shown in the IC wafer 12, whereas typically as many as six or more levels may be used. The package further includes an intermediate wafer 20 having one or more intermediate contact pads 22. The intermediate contact pads 22 are connected to an electro-optic arrangement 24 on the intermediate wafer 20. As will be discussed in greater detail below, after fabrication is complete, the contact pads 14, 22 form a plurality of direct copper bonds such that the gap between the two wafers 12, 20 is eliminated. By eliminating the gap between the two wafers 12, 20, a number of performance difficulties can be obviated.

[0016] Specifically, the illustrated embodiment of the electro-optic arrangement includes a first arrangement 24a and a second arrangement 24b. The first arrangement 24a has a waveguide 26 disposed within the intermediate wafer 20. An optical coupler 28 is positioned adjacent to the waveguide 26 within the intermediate wafer 20 such that the coupler 28 enables receipt of an optical signal from the waveguide 26. The optical signal can be obtained from any source such as a laser, light emitting diode (LED) or another waveguide. It will be appreciated that the source of the optical signal may also originate from within the intermediate wafer 20 or from an external source. An electro-optic converter such as optical detector 30 is positioned between the optical coupler 28 and one or more of the intermediate contact pads 22 such that the optical detector 30 enables transfer of an electrical signal to the intermediate contact pads based on the optical signal. Optical detectors are well documented in the semiconductor industry and any number of commercially available detectors can be used. In the illustrated embodiment, the optical detector 30 enables transfer of the electrical signal to intermediate contact pads 22b and 22c. The resulting electrical signal may be a clock signal, input/output (I/O) signal, or any other type of signal suitable for transmission in the optical domain. It should be noted, however, that clock and I/O signals typically contain higher frequencies and therefore lend themselves to optical transmission due to bandwidth concerns.

[0017] It will further be appreciated that the number, orientation and positioning of the intermediate contact pads 22 depends upon the architecture of the electro-optic arrangement 24 and the particular application in which the semiconductor package 10 is used. It can further be seen that the second arrangement 24b similarly includes a waveguide 32 disposed within the intermediate wafer 20, and an optical coupler 34. The optical coupler 34 is positioned adjacent to the waveguide 32 within the intermediate wafer 20 and enables transmission of an optical

signal to the waveguide 32. An electro-optic converter such as optical emitter 36 is positioned between the optical coupler 34 and intermediate contact pads 22e and 22f such that the optical emitter 36 enables transfer of an optical signal to the waveguide 32 based on the electrical signal transported by the intermediate contact pads 22e and 22f. It can be seen that the waveguide 32 extends to an external surface of the intermediate wafer 20 in order to demonstrate the possibility of sending optical signals to external components. Waveguide 26, on the other hand, is shown as extending in a direction that is perpendicular to the waveguide 32 and illustrates the possibility of using other internal light sources. Thus, the electro-optic arrangement 24 can include optical detectors 30, optical emitters 36, or any combination thereof without parting from the spirit and scope of the invention.

[0018] It can further be seen that the illustrated intermediate wafer 20 further includes vias 38, 40 that extend through the intermediate wafer 20 to intermediate contact pads 22a and 22d. The vias 38, 40 provide a mechanism for testing certain locations or interconnecting the semiconductor package 10 with other structures such as pin grid arrays (PGAs), ball grid arrays (BGAs), etc. Additionally, the semiconductor package 10 provides a mechanism for facilitating manipulation of the package 10 by personnel, fabrication machinery and other external elements. Specifically, the intermediate wafer 20 may be built upon or attached to a handle wafer 44, by means of a release layer 42. The handle 44 is removable by etching away the release layer 42 after the direct copper bonding process as best shown in FIG. 2.

[0019] Turning now to FIG. 3, a method of fabricating an electro-optic semiconductor package is shown at 50 in accordance with one embodiment of the present invention. Generally, an IC wafer having one or more IC contact pads is provided at processing block 52. As already discussed, the IC contact pads are connected to an IC on the IC wafer. An intermediate wafer

having one or more intermediate contact pads is provided at block 54, where the intermediate contact pads are connected to an electro-optic arrangement on the intermediate wafer. Processing block 56 provides for direct copper bonding the IC contact pads to adjacent intermediate contact pads such that the electro-optic semiconductor package results. In the preferred embodiment, the release layer is removed at block 58 in order to facilitate connection to any vias that may be present.

[0020] FIG. 4 illustrates the preferred approach to direct copper bonding the contact pads in greater detail at block 56. Specifically, the IC contact pads and the intermediate contact pads are cleaned at block 60. One approach to the cleaning process is to use an acid bath followed by a water rinse and spin-dry. Applicable cleaning processes are discussed in greater detail in "Copper Wafer Bonding", A. Fan et al., *Electrochemical and Solid State Letters*, 2 (10), pp. 534-36 (1999). Although the purpose of the acid bath is to remove any native oxide that exists on the metal surface of the contact pads, it has been determined that wafer bonding without surface preparation can also be achieved with reproducible results. Notwithstanding, processing block 62 provides for disposing the IC contact pads adjacent to the intermediate contact pads in an oxidation-resistant environment (such as nitrogen) having a predetermined ambient temperature. While the appropriate ambient temperature varies based on a number of factors, temperatures on the order of 390 °C have been demonstrated as being sufficient to support the bonding process. The IC contact pads are forced into direct contact with the adjacent intermediate contact pads at a predetermined pressure for a predetermined period of time at processing block 64 such that a direct copper bond results. It should be noted that as a result of the above-described process, adjacent contact pads become a single, continuous layer of copper as opposed to the copper-solder-copper interface obtained from C4 bonding and other conventional approaches. It should

also be noted that the use of such a bond to reduce both optical and electrical losses represents a significant improvement over traditional approaches. Key performance metrics associated with direct copper bonding are discussed in "Comparison of Key Performance Metrics in Two-and Three-Dimensional Integrated Circuits", A. Rahman et al., *Microsystems Technology*, MIT, Cambridge, MA.

[0021] Indeed, FIG. 5 demonstrates that the direct copper bond enables a unique approach to fabricating the intermediate wafer. For example, fabrication method 66 includes the processing block 68 of disposing a waveguide within the intermediate wafer. An optical coupler is positioned adjacent to the waveguide within the intermediate wafer at block 70 such that the coupler enables receipt of an optical signal from the waveguide. Processing block 72 provides for positioning an optical detector between the optical coupler and one or more intermediate contact pads of the intermediate wafer such that optical detector enables transfer of an electrical signal to the intermediate contact pads based on the optical signal. Thus, the optical detector can be placed on the intermediate wafer as opposed to the conventional approach of placing the detector on the IC wafer. By so doing, a number of advantages can be achieved. For example, the optical losses that normally occur as a result of the C4 gap between the wafers are minimized. Furthermore, the electrical losses associated with transmitting electrical signals across the C4 bond are significantly reduced. Such losses include unwanted interconnect delay, resistance, capacitance, and loop inductance. It can further be seen that vias are extended through the intermediate wafer to one or more of the intermediate contact pads at block 74.

[0022] It should be noted that the order in which many of the processes described herein are preformed may vary depending on the circumstances. For example, manufacturing concerns may dictate that the vias be created before disposition of the waveguide, or that the optical

detector be positioned before placement of the waveguide and optical coupler. It is also possible that the release layer is deposited on the handle wafer and the intermediate wafer 20 is built up over the handle wafer. In this approach, a base cladding layer would first be deposited, followed by deposition and definition of the waveguide material. The optical coupler 34 is defined, followed by the deposition and definition of the optical detector, and finally through via 40 definition and intermediate contact pad 22 definition.

[0023] Those skilled in the art can now appreciate from the foregoing description that the broad teachings of the present invention can be implemented in a variety of forms. Therefore, while this invention has been described in connection with particular examples thereof, the true scope of the invention should not be so limited since other modification will become apparent to the skilled practitioner upon a study of the drawings, specification, and following claims.

It is claimed that:

1. A method of fabricating an electro-optic semiconductor package, the method comprising:

providing an integrated circuit (IC) wafer having one or more IC contact pads, the IC contact pads being connected to an IC on the IC wafer;

providing an intermediate wafer having one or more intermediate contact pads, the intermediate contact pads being connected to an electro-optic arrangement on the intermediate wafer; and

direct copper bonding the IC contact pads to adjacent intermediate contact pads, the electro-optic semiconductor package resulting.

2. The method of claim 1 further including:

cleaning the contact pads;

disposing the IC contact pads adjacent to the intermediate contact pads in an oxidation-resistant environment having a predetermined ambient temperature; and

forcing the IC contact pads into direct contact with the adjacent intermediate contact pads at a predetermined pressure, a direct copper bond resulting.

3. The method of claim 2 further including cleaning the contact pads in an acid bath.

4. The method of claim 2 further including disposing the IC contact pads adjacent to the intermediate contact pads in a nitrogen environment.

5. The method of claim 1 further including:

disposing a waveguide within the intermediate wafer;

positioning an optical coupler adjacent to the waveguide within the intermediate wafer, the coupler enabling transport of an optical signal and the intermediate contact pads enabling transport of an electrical signal; and

positioning an electro-optic converter between the optical coupler and one or more of the intermediate pads, the converter enabling conversion between the optical signal and the electrical signal.

6. The method of claim 5 further including positioning an optical detector between the optical coupler and one or more of the intermediate pads, the detector enabling conversion of the optical signal into the electrical signal.

7. The method of claim 5 further including positioning an optical emitter between the optical coupler and one or more of the intermediate pads, the emitter enabling conversion of the electrical signal into the optical signal.

8. The method of claim 5 further including extending a via through the intermediate wafer to one or more of the intermediate contact pads.

9. The method of claim 5 further including:

coupling a release layer to a surface of the intermediate wafer; and

coupling a handle to the release layer.

10. The method of claim 9 further including removing the release layer after direct copper bonding the IC contact pads to the intermediate contact pads.

11. The method of claim 10 further includes etching away the release layer.

12. The method of claim 5 further including enabling conversion between the optical signal and a clock signal.

13. The method of claim 5 further including enabling conversion between the optical signal and an input/output (I/O) signal.

14. The method of claim 1 further including providing a computer processor wafer having one or more IC contact pads.

15. The method of claim 1 further including providing a chip interposer as the intermediate wafer.

16. The method of claim 1 further including providing a host wafer as the intermediate wafer.

17. A method of fabricating an intermediate wafer, the method comprising:

disposing a waveguide within the intermediate wafer;

positioning an optical coupler adjacent to the waveguide within the intermediate wafer, the coupler enabling transport of an optical signal and one or more intermediate contact pads of the intermediate wafer enabling transport of an electrical signal; and

positioning an electro-optic converter between the optical coupler and the intermediate contact pads, the converter enabling conversion between the optical signal and the electrical signal.

18. The method of claim 17 further including positioning an optical detector between the optical coupler and one or more of the intermediate pads, the detector enabling conversion of the optical signal into the electrical signal.

19. The method of claim 17 further including positioning an optical emitter between the optical coupler and one or more of the intermediate pads, the emitter enabling conversion of the electrical signal into the optical signal.

20. The method of claim 17 further including:

coupling a release layer to a surface of the intermediate wafer; and

coupling a handle to the release layer.

21. The method of claim 20 further including removing the release layer after direct copper bonding one or more IC contact pads to the intermediate contact pads.

22. The method of claim 21 further including etching away the release layer.

23. A method of fabricating an electro-optic semiconductor package, the method comprising:

providing a processor wafer having one or more IC contact pads, the IC contact pads being connected to a computer processor on the processor wafer;

coupling a release layer to a surface of an intermediate wafer;

coupling a handle to the release layer;

disposing a waveguide within the intermediate wafer;

positioning an optical coupler adjacent to the waveguide within the intermediate wafer, the coupler enabling receipt of an optical signal from the waveguide;

positioning optical detector between the optical coupler and one or more intermediate contact pads, the optical detector enabling transfer of an electrical signal to the intermediate contact pads based on the optical signal;

cleaning the contact pads in an acid bath;

disposing the IC contact pads adjacent to the intermediate contact pads in an oxidation-resistant environment having a predetermined ambient temperature; and

forcing the IC contact pads into direct contact with the intermediate contact pads at a predetermined pressure, a direct copper bond resulting.

24. The method of claim 23 further including removing the release layer after direct copper bonding the IC contact pads to the intermediate contact pads.

25. The method of claim 24 further including etching away the release layer.

26. An electro-optic semiconductor package comprising:

an integrated circuit (IC) wafer having one or more IC contact pads, the IC contact pads being connected to an IC on the IC wafer;

an intermediate wafer having one or more intermediate contact pads, the intermediate contact pads being connected to an electro-optic arrangement on the intermediate wafer; and

said contact pads forming a plurality of direct copper bonds.

27. The package of claim 26 wherein the electro-optic arrangement of the intermediate wafer includes:

a waveguide disposed within the intermediate wafer;

an optical coupler positioned adjacent to the waveguide within the intermediate wafer, the coupler enabling receipt of an optical signal from the waveguide; and

an optical detector positioned between the optical coupler and one or more of the intermediate contact pads, the optical detector enabling transfer of an electrical signal to the intermediate contact pads based on the optical signal.

28. The package of claim 27 wherein the intermediate wafer further includes a via extending through the intermediate wafer to one or more of the intermediate contact pads.

29. The package of claim 26 further including:

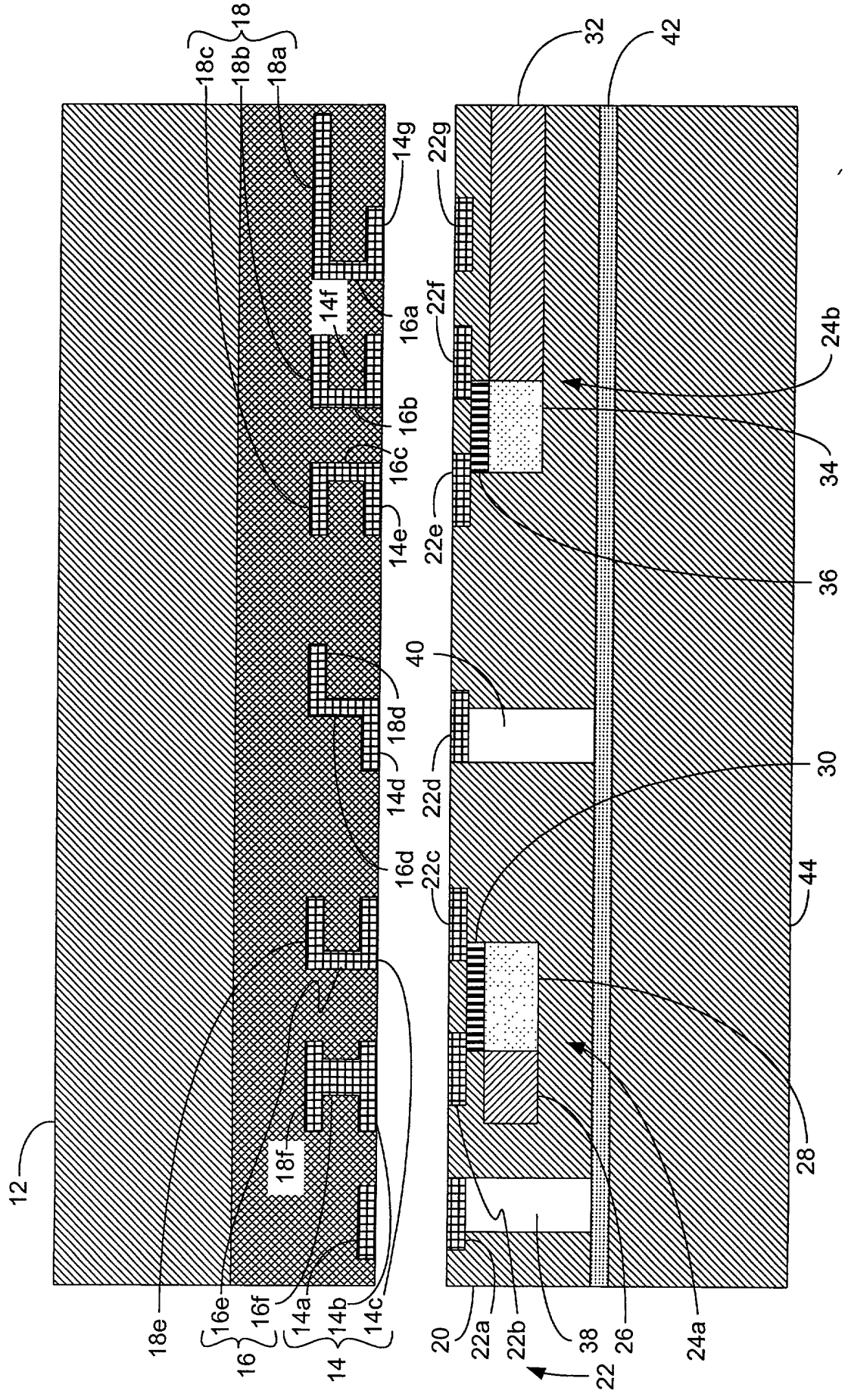
a release layer coupled to a surface of the intermediate wafer; and

a handle coupled to the release layer.

30. The package of claim 29 wherein the handle is removable by etching away the release layer.

ABSTRACT OF THE DISCLOSURE

An electro-optic semiconductor package and fabrication method provides enhanced performance. An integrated circuit (IC) having one or more IC contact pads is provided, where the IC contact pads are connected to an IC on the IC wafer. An intermediate wafer having one or more intermediate contact pads is provided, where the intermediate contact pads are connected to an electro-optic arrangement on the intermediate wafer. The method further provides for direct copper bonding the IC contact pads to adjacent intermediate contact pads such that an electro-optic semiconductor package results.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14d
22d
30
16d
22c
44
12
18f
28
18e
16e
16f
14a
14b
14c
16
14
20
22a
22b
38
26
24a
22

FIG. 1

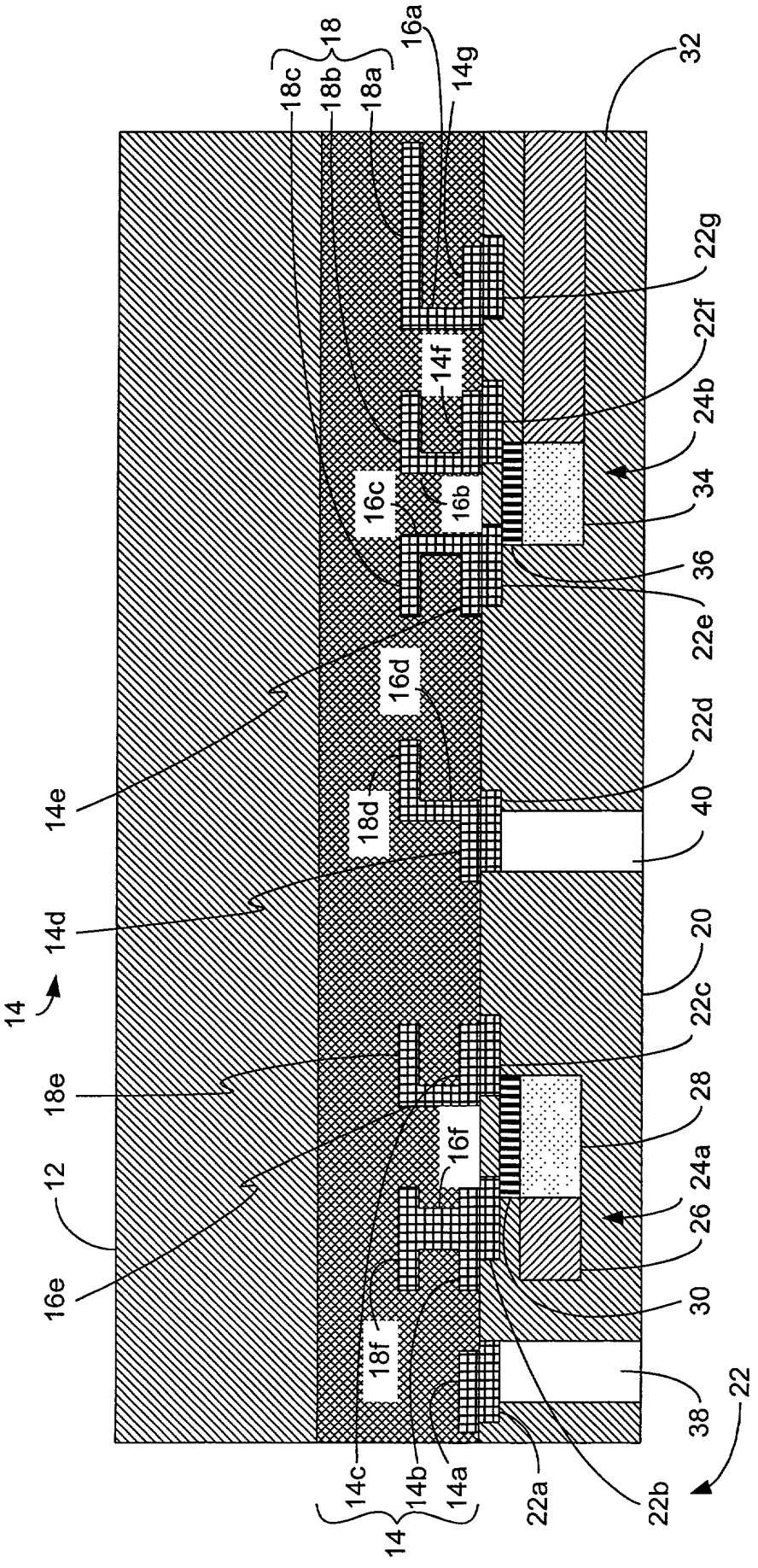
10
12
14
14a
14b
14c
14d
14e
14f
14g
16a
16b
16c
16d
16e
16f
18
18a
18b
18c
18d
18e
18f
20
22
22a
22b
22c
22d
22e
22f
22g
24a
24b
26
28
30
32
34
36
38
40

FIG. 2

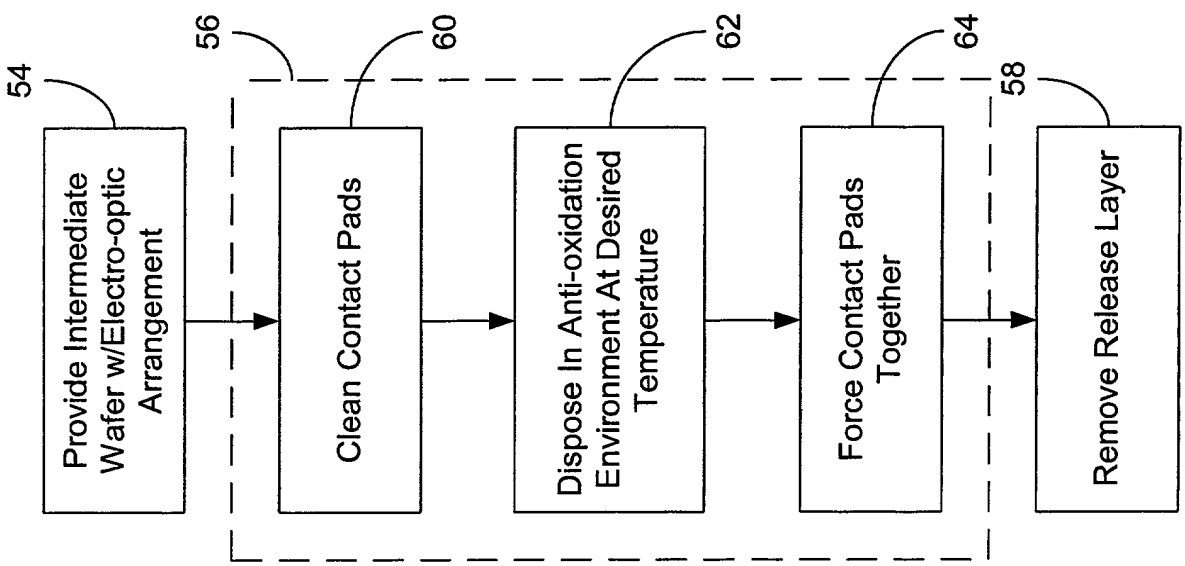
54
56
60
62
64
58
Provide Intermediate Wafer w/Electro-optic Arrangement
Clean Contact Pads
Dispose In Anti-oxidation Environment At Desired Temperature
Force Contact Pads Together
Remove Release Layer

FIG. 4

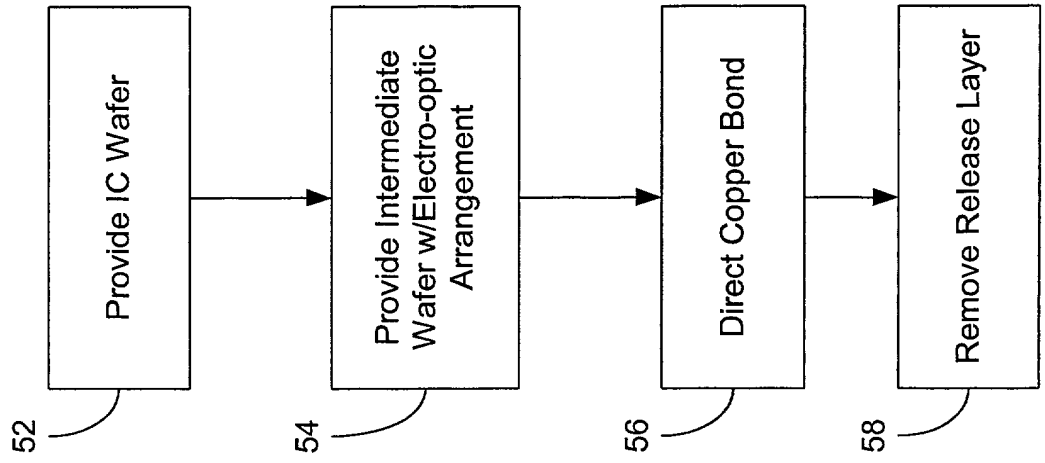
50
Provide IC Wafer
Provide Intermediate Wafer w/Electro-optic Arrangement
Direct Copper Bond
Remove Release Layer
52
54
56
58

FIG. 3

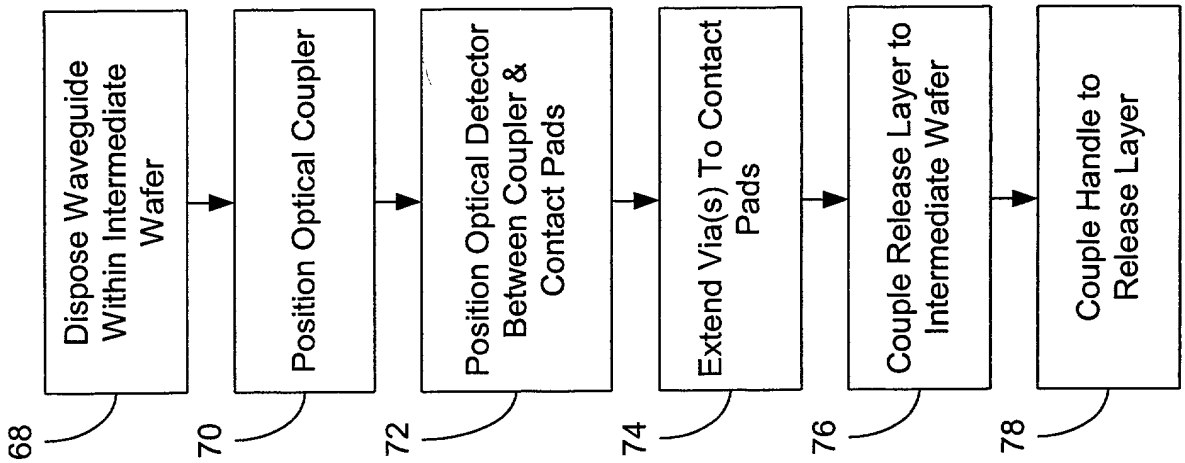
66
Dispose Waveguide Within Intermediate Wafer
68
Position Optical Coupler
70
Position Optical Detector Between Coupler & Contact Pads
72
Extend Via(s) To Contact Pads
74
Couple Release Layer to Intermediate Wafer
76
Couple Handle to Release Layer
78

FIG. 5

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DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ELECTRICAL/OPTICAL INTEGRATION SCHEME USING DIRECT COPPER BONDING

the specification of which is attached hereto unless the following is entered:

was filed on	as United States Application Number or PCT International Application Number	and was amended on (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR ' 1.56.

PRIOR FOREIGN APPLICATION(S)

I hereby claim foreign priority benefits under 35 USC ' 119(a-d) or ' 365(b) of any foreign application(s) for patent or inventor=s certificate, or ' 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application(s) for patent or inventor=s certificate, or PCT international application having a filing date before that of the application on which priority is claimed:

Application Number	Country	Filing Date (day/month/year)	Priority Not Claimed

PROVISIONAL APPLICATION(S)

I hereby claim the benefit under 35 USC ' 119(e) of any United States provisional application(s) listed below:

Application Number		Filing Date	

PRIOR UNITED STATES APPLICATION(S)

I hereby claim the benefit under 35 USC ' 120 of any United States application(s), or ' 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 USC ' 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR ' 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

Application Number	Filing Date	Status (patented, pending, abandoned)

POWER OF ATTORNEY

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (Cont.)

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I hereby declare that all statements made herein of my own knowledge are true and all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under ' 1001 of Title 18 of the United States Code and that such willful statements may jeopardize the validity of the application or any patent issuing thereon.

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Signature		Date	
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Residence	City	State or Country	Country of Citizenship
Post Office Address	Street	City	State or Country & Zip Code
Signature		Date	